Amendments to the claims:

1 (Currently Amended) A digital gain control system comprising:

an rms voltage converter receiving one or more digital inputs and forming an rms value; and

a digital gain controller including:

an iteration variable set to an initial value;

a digital gain value having n data bits, said digital gain value having a maximum value and a minimum value, the initial digital gain value being set to the median of said maximum value and said minimum value;

a correction value having an initial value which is half of said initial digital gain value;

an iteration controller which performs the following sequential steps m times, said m being an integer less than said n:

comparing the rms value from said rms voltage converter to a threshold voltage value;

adding said correction value to said digital gain value if said rms value is less than said threshold voltage value, or subtracting said correction value from said digital gain value if said rms value is greater than said threshold voltage value;

forming a new correction value for a subsequent iteration by halving said correction value.

2 (Previously Amended) The digital gain control system of claim 1 wherein said m is a system constant derived from:

Nbinary, the number of search bits;

η, the dB/step gain of a receiver to be controlled by said digital gain value;

Ndata, the bitwidth of the output of an A/D converter sampling a signal amplified by a variable gain amplifier, said variable gain controlled by said digital gain value;

κ, the number of A/D converters quantization steps required for digital signal processing.

3 (Previously Amended) The digital gain control system of claim 2 wherein said m is computed from:

$m = \text{Nbinary} - [\log_2(10*\log_{10}((2^{\text{Ndata}}-1)/\kappa\eta) + 1]$,

and the operator [.] rounds down to an integer value.

4 (Previously Amended) The digital gain control system of claim 1 wherein said correction value is $2^{(n-k-1)}$,and said k is the number of times said iteration has been performed.

5 (Previously Amended) The digital gain control system of claim 1 wherein said correction value is positive.

6 (Previously Amended) The digital gain control system of claim 1 wherein said correction value is negative.

7 (Previously Amended) The digital gain control system of claim 1 wherein said iteration controller operates over a duration of time substantially equal to the duration of a received packet, said packet including a first interval and a second interval, the time duration between at least one said iteration during said first interval being less than the time duration between at least one said iteration during said second interval.

8 (Previously Amended) The digital gain control system of claim 7 wherein said first interval corresponds to a preamble interval of a wireless Ethernet packet.

9 (Previously Amended) The digital gain control system of claim 7 wherein said second interval corresponds to a payload interval following said first interval in a wireless Ethernet packet.

10 (Currently Amended) A process for generating a value Vagc where said Vagc is a digital value having n bits and

operative for controlling the gain of a processor which produces one or more channels of digital samples, said process comprising:

setting Vagc to an initial value;

setting Vcorrection to a value substantially equal to half of said Vagc initial value; and

performing the following first through fourth steps m iterations in sequence:

a first step of measuring said digital samples;

a second step of converting said digital samples into an rms value;

a third step of comparing said rms value with a threshold value and adding said Vcorrection to said Vagc if said rms value is less than said threshold value, and subtracting said Vcorrection from said Vagc if said rms value is greater than said threshold value;

a fourth step of forming a new value of said Vcorrection by halving the value of said Vcorrection.

11 (Previously Amended) The process of claim 10 wherein said m is a system constant derived from:

Nbinary, the number of search bits;

η, the dB/step gain of a receiver to be controlled by said digital gain value;

Ndata, the bitwidth of the output of an A/D converter sampling a signal amplified by a variable gain amplifier, said variable gain controlled by said digital gain value;

κ, the number of A/D converter quantization steps required for digital signal processing.

12 (Previously Amended) The process of claim 10 wherein said Vagc has a maximum value of 2^n-1.

13 (Previously Amended) The process of claim 10 wherein said gain correction value is $2^{(n-k-1)}$, and k is the number of the iteration, starting at 1 and incrementing by 1 for each said iteration.

14 (Previously Amended) The process of claim 10 wherein said Vcorrection value is positive.

15 (Previously Amended) The process of claim 10 wherein said Vcorrection value is negative.

16 (Previously Amended) The process of claim 10 wherein said first through fourth steps comprise an iteration time wherein the iteration time during a first interval is shorter than the iteration time during a second interval and wherein the second interval follows said first interval.

17 (Previously Amended) The process of claim 16 wherein said first interval corresponds to a preamble time T1 of a wireless Ethernet packet.

18 (Previously Amended) The process of claim 16 wherein said second interval corresponds to a frame time following the preamble time of a wireless Ethernet packet.

19 (Previously Amended) The process of claim 10 wherein said m iterations occurs during a preamble time of a wireless Ethernet packet.

20 (Currently Amended) An RF front end comprising:

an RF receiver responsive to a digital gain control input of width n bits, said RF receiver producing quadrature output digital values; and

a digital gain controller coupled to said digital gain control input and producing a digital output Vagc coupled to said digital gain control input in response to said quadrature output digital values, said output Vagc generated by:

setting Vagc to an initial value $2^{(n-1)}-1$ and setting an iteration variable k to 0;

performing the following first through fourth steps while said k is less than m, where said m is an integer less than said n:

a first step of measuring said quadrature output digital values and producing the rms value of said quadrature output digital values;

a second step of comparing said rms value to a threshold value;

a third step of incrementing said k;

a fourth step of adding a correction value $2^{(n-k-1)}$ to said Vagc if said rms value is less than said threshold value, and subtracting a correction value $2^{(n-k-1)}$ from said Vagc if said rms value is greater than said threshold value.

21 (Previously Amended) The RF front end of claim 20 wherein said m is a system constant derived from:

Nbinary, the number of search bits;

η, the dB/step gain of a receiver to be controlled by said digital gain value;

Ndata, the bitwidth of the output of an A/D converter sampling a signal amplified by a variable gain amplifier, said variable gain controlled by said digital gain value;

κ, the number of A/D converters quantization steps required for digital signal processing.

22 (Previously Amended) The RF front end of claim 20 wherein said correction value is positive.

23 (Previously Amended) The RF front end of claim 20 wherein said correction value is negative.

24 (Previously Amended) The RF front end of claim 20 wherein said first through fourth steps comprise an iteration time wherein the iteration time during a first interval is shorter than the iteration time during a second interval and wherein the second interval follows said first interval.

25 (Previously Amended) The RF front end of claim 24 wherein said first interval corresponds to a preamble time of a wireless Ethernet packet.

26 (Previously Amended) The RF front end of claim 24 wherein said second interval corresponds to a frame time following the preamble time of a wireless Ethernet packet.

27 (Currently Amended) The RF front end of claim 20 wherein said ~~m times occurs~~ first through fourth steps occur during a preamble time of a wireless Ethernet packet.

28 (Currently Amended) A digital gain control system for a first and second stream of quadrature data, said first and said second stream of quadrature data multiplexed into a single alternating stream of data having an associated first stream interval and a second stream interval, the digital gain control system operative on said single stream of data and computing a gain control value ~~from~~ for each said first and said second stream of quadrature data ~~using a single hardware function comprising~~ said digital gain control system including:

an rms voltage converter receiving one or more ~~digital inputs and~~ values from said single stream of data and forming an rms value; and

a digital gain controller ~~having~~ including:

an iteration variable associated with each said stream of data, each said iteration variable set to an initial value;

a digital gain value for each said stream of data, each said digital gain value having n bits, said digital gain value having a maximum value and a minimum value, each said digital gain value being initially set to the median of said maximum value and said minimum value;

a correction value associated with each said stream of data, each said correction value having an initial value which is substantially half of the initial digital gain value associated with a corresponding said stream of data;

an iteration process which performs the following sequential steps m times for each said stream of data:

comparing the rms value from said rms voltage converter for a particular stream of data to a threshold voltage value associated with said particular stream of data;

adding said correction value associated with said particular stream of data to said digital gain value if said rms value is less than said threshold voltage level associated with said particular stream of data, or subtracting said correction value associated with said particular stream of data from said digital gain value if said rms value is greater than said threshold voltage level associated with said particular stream of data;

forming a new correction value associated with said particular stream of data by halving said correction value associated with said particular stream of data;

whereby ~~said hardware function computes a~~ said digital gain control systems computes said first gain control value using only values from said first stream of data and computes said second gain control value using only values from said second stream of data. ~~value for each of said first and said second stream of quadrature data.~~

29 (Currently Amended) The system of claim 28 wherein the iteration time for a particular said stream of data during a first interval is shorter than the iteration time during a second interval for said particular stream of data and wherein the second interval follows said first interval.

30 (Currently Amended) The system of claim ~~28~~ 29 where said first interval corresponds to a preamble time of a wireless Ethernet packet.

31 (Currently Amended) The system of claim ~~28~~ 29 where said second interval corresponds to a frame time following the preamble time of a wireless Ethernet packet.

32 (Previously Amended) The system of claim 28 where said m times occurs during a preamble time of a wireless Ethernet packet.

33 (Currently Amended) An RF front end comprising:

a first RF receiver having a digital gain control input of width n and producing a first quadrature output digital value including a first I value and a first Q value;

a second RF receiver having a digital gain control input of width n bits and producing a second quadrature output digital value including a second I value and a second Q value;

a multiplexer converting said first I value and said second I value into a stream of alternating first and second I values, and also converting said first Q value and said second Q value into a stream of alternating first and second Q values; and

a digital gain controller coupled to said stream of alternating I values and said stream of alternating Q values and producing a first output Vagc and a second output Vagc, respectively, each of said first Vagc and said second Vagc independently generated by:

setting Vagc to an initial value $2^{(n-1)}-1$, where n is said bit width, and setting an iteration variable k to 0;

performing the following steps while said k is less than said m:

a first step of measuring said quadrature digital values and producing the rms value of said quadrature digital values;

a second step of comparing said rms value to a threshold value;

a third step of incrementing said k; and

a fourth step of adding a correction value $2^{(n-k-1)}$ to said Vagc if said rms value is less than said threshold value, and subtracting the correction value $2^{(n-k-1)}$ from said Vagc if said rms value is ~~less~~ greater than said threshold value. ~~value;~~

34 (Previously Amended) The RF front end of claim 33 wherein said first through fourth steps comprise an iteration time wherein the iteration time during a first interval is shorter than the iteration time during a second interval and wherein the second interval follows said first interval.

35 (Previously Amended) The RF front end of claim 34 wherein said first interval corresponds to a preamble time of a wireless Ethernet packet.

36 (Previously Amended) The RF front end of claim 34 wherein said second interval corresponds to a frame time following the preamble time of a wireless Ethernet packet.

37 (Previously Amended) The RF front end of claim 34 wherein said first through fourth steps occur during a preamble time of a wireless Ethernet packet.

38 (Currently Amended) A process for generating a first value Vagc and a second value Vagc from an alternating stream of first quadrature data and second quadrature data, where said first Vagc is derived exclusively from said first quadrature data and said second Vagc is derived exclusively from said second quadrature data, where each of said first Vagc and said second Vagc are each digital values having n bits, said process comprising for each said first and second Vagc:

setting Vagc to a first value; and

setting Vcorrection to a value equal to substantially half of said Vagc first value;

performing the following steps m times in sequence:

measuring one or more said quadrature data samples and converting said quadrature data samples into an rms value;

comparing said rms value with a threshold value and

adding said Vcorrection to said Vagc if said rms value is less than said threshold value, and subtracting said Vcorrection from said Vagc if said rms value is greater than said threshold value;

forming a new value of said Vcorrection by halving the value of said Vcorrection.

39 (Previously Amended) The process of claim 38 wherein said first through fourth steps have an iteration time wherein the iteration time during a first interval is shorter than the iteration time during a second interval and wherein the second interval follows said first interval.

40 (Previously Amended) The process of claim 38 wherein said first interval corresponds to a preamble time of a wireless Ethernet packet.

41 (Previously Amended) The process of claim 38 wherein said second interval corresponds to a frame time following the preamble time of a wireless Ethernet packet.

42 (Previously Amended) The process of claim 38 wherein said m times occurs during a preamble time of a wireless Ethernet packet.

43 (Previously Presented) The process of claim 1 wherein said m is one of the values 3, 4, or 5.

44 (Previously Presented) The process of claim 11 wherein said m is one of the values 3, 4, or 5.

45 (Previously Presented) The process of claim 21 wherein said m is one of the values 3, 4, or 5.

46 (Previously Presented) The process of claim 11 whereby said m is computed from:

$m = Nbinary - [\log_2(10*\log_{10}((2^{Ndata}-1)/\kappa\eta) + 1]$

and the operator [.] rounds down to an integer value.

47 (Previously Presented) The process of claim 21 whereby said m is computed from:

$m = Nbinary - [\log_2(10*\log_{10}((2^{Ndata}-1)/\kappa\eta) + 1]$ and the operator [.] rounds down to an integer value.